REMARKS

Claims 1, 3 and 7 are rejected as being anticipated under 35 U.S.C. 102(e) by Rhee, *et al.* (United States Patent Number 6,774,712). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Bae, *et al.* (United States Patent Number 6,373,754). Claims 33, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Park, *et al.* (United States Patent Number 5,349,559). Claims 10-12, 14-17, 23, 25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (United States Publication Number 2002/0053943) in view of Sher (United States Patent Number 6,633,196). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections is respectfully requested.

With regard to claim 17, claim 17 was previously withdrawn. Removal of the rejection of claim 17 based on Yamasaki is respectfully requested.

Independent claim 10 is amended herein to clarify that a switching circuit is coupled to both a control signal generating circuit and an output of a comparing circuit for receiving a control signal and for transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated.

With regard to the rejection of claims 1, 3, and 7 based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal

indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 1.

Rhee, *et al.* teaches a circuit that generates an internal voltage source (IVC) in a first operating mode (or normal operating mode) when a control signal PDPDE is "low" and a complementary control signal PDPDEB is "high" (see Rhee, Figure 1, column 3, lines 24-30, and column 4, lines 20-27), and converts the first operating mode into a second operating mode when the control signal PDPDE becomes "high" and the complementary control signal PDPDBB becomes "low" (see Rhee, Figure 1 and column 4, lines 33-36). However, contrary to statements made in the Office Action at page 2, the outputted complementary control signal PDPDEB as well as the control signal PDPDE (which is not referred to in the Office Action) of Rhee, *et al.* are different than the control signal generating circuit, as claimed in claim 1, since there is no teaching or suggestion in Rhee, *et al.* of either the outputted complementary control signal PDPDEB or the control signal PDPDE being a control signal that is generated by a control signal generating circuit and that is responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 1. Instead, the circuit disclosed in Rhee, *et al.* generates the IVC regardless of a number of bits, similar to the conventional circuit described in the Background of the Invention section of the present specification at pages 2-3, paragraphs [0008] – [0010].

In addition, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when a control signal is inactivated, wherein the comparing circuit comprises a comparator connected between a first node and a ground voltage and comparing a reference voltage to an internal

voltage to generate the driving signal and a switching circuit connected between an external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated, as claimed in amended independent claim 1.

This difference between the present invention as claimed in claim 1 and Rhee, *et al.* can be best described by way of illustration. In an embodiment illustrated at Figure 5 of the present specification, a comparing circuit comprises a comparator 10 connected between a first node and a ground voltage, and a switching circuit 40 connected between an external power voltage EVC and the first node that cuts off the external power voltage EVC applied to the comparator 10 when a control signal C is activated. Rhee, *et al.*, on the other hand, discloses a differential amplifier 52 (referred to in the Office Action at page 3, line 5 as a comparator) and a PMOS transistor 58 (referred to in the Office Action at page 3, line 7 as a switching circuit) (see Rhee, Figure 4). However, there is no teaching or suggestion in Rhee, *et al.* of the differential amplifier 52 being connected between a first node and a ground voltage, as claimed in claim 1. Nor is there is no teaching or suggestion in Rhee, *et al.* of the PMOS transistor 58 being connected between an external power voltage and the first node, as claimed in claim 1. In sum, there is no teaching or suggestion in Rhee, *et al.* of the differential amplifier 52 and the PMOS transistor 58 both being connected to a first node.

For at least the reasons described herein, it is submitted that Rhee, *et al.* fails to teach or suggest the invention set forth in the amended claims. Reconsideration of the rejections of claims 1, 3, and 7 under 35 U.S.C. 102(e) based on Rhee, *et al.* is respectfully requested.

With regard to dependent claims 7-9 and 30-32, Applicants note that the Office Action Summary indicates that claims 7-9 and 30-32 are rejected, but there is no specific rejection made with regard to claims 7-9 and 30-32. However, the Office Action at page 3 indicates that claims 7-9 and 30-32 are "deemed to be intended use." Applicants assume that claims 7-9 and 30-32 are rejected for being statements of intended use. Accordingly, claims 7, 8, and 30-32 are

amended in a manner that is believed to overcome the assumed rejection of claims 7, 8, and 30-32. No new matter is added. With regard to claim 9, Applicants submit that claim 9 is not a statement of intended use, but, rather, is a limitation that recites a structural component of the present invention, that is, an "input signal" that is a "mode setting signal comprising a plurality of mode setting bits." Reconsideration and removal of the assumed rejection of claims 7-9 and 30-32 are respectfully requested.

Applicants further note that claims 14-16 and 27-29 are amended above in a similar manner as claims 7-9.

With regard to independent claims 34, 35, and 37, the Office Action at page 4, line 3 refers to claims 34, 35, and 37 as also being rejected. Applicants assume that claims 34, 35, and 37 are rejected under 35 U.S.C. 102(e) based on Rhee, *et al.*

In view of the foregoing assumption, with regard to claim 34, Applicants submit that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 34, for reasons similar to those described above with regard to independent claim 1. In addition, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit comprises a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, as claimed in

independent claim 34, for reasons similar to those described above with regard to independent claim 1.

With regard to claim 35, it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal according to a number of data bits, as claimed in independent claim 35, for reasons similar to those described above with regard to independent claim 1. In addition, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes a comparator connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated, as claimed in independent claim 35, for reasons similar to those described above with regard to independent claim 1.

With regard to claim 37, it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal according to a number of data bits, as claimed in independent claim 37, for reasons similar to those described above with regard to independent claim 1. In addition, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claim 37, for reasons similar to those described above with regard to independent claim 1.

With regard to the rejection of claim 2 based on the combination of Rhee, *et al.* and

Bae, *et al.*, it is submitted that Bae, *et al.*, like Rhee, *et al.*, fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 1. In addition, it is submitted that Bae, *et al.*, like Rhee, *et al.*, fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when a control signal is inactivated, wherein the comparing circuit comprises a comparator connected between a first node and a ground voltage and comparing a reference voltage to an internal voltage to generate the driving signal and a switching circuit connected between an external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated, as claimed in amended independent claim 1.

Since neither Rhee, *et al.* nor Bae, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Rhee, *et al.* and Bae, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in claim 1, claim 2, which depends on claim 1, is believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claim 2 under 35 U.S.C. 103(a) based on Rhee, *et al.* and Bae, *et al.* is respectfully requested.

With regard to the rejection of independent claims 33, 36, and 38 based on Rhee, *et al.* and Park, *et al.*, it is submitted that neither Rhee, *et al.* nor Park, *et al.* teaches or suggests a control signal generating circuit for generating a control signal responsive to an input signal

related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 33, or a control signal generating circuit for generating a control signal according to a number of data bits, as claimed in independent claims 36 and 38. In addition, it is submitted that neither Rhee, *et al.* nor Park, *et al.* teaches or suggests a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when a control signal is inactivated, wherein the comparing circuit comprises a comparator connected between a first node and a second node and comparing the reference voltage to the internal voltage to generate the driving signal, a first switching circuit connected between an external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated, and a second switching circuit connected between the second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claim 33 and 36.

Since neither Rhee, *et al.* nor Park, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Rhee, *et al.* and Park, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in claim 33, 36, and 38, claims 33, 36, and 38 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claim 33, 36, and 38 under 35 U.S.C. 103(a) based on Rhee, *et al.* and Park, *et al.* is respectfully requested.

With regard to the rejection of independent claim 10 based on the combination of Yamasaki, *et al.* and Sher, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or

suggests a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 10.

Yamasaki, *et al.* teaches a portion of a semiconductor memory device that includes a voltage down converter VDC, a driving circuit 2 (see Yamasaki, Figure 1), and a test mode setting circuit (see Yamasaki, Figure 5). The voltage down converter VDC is a conventional voltage down converter VDC, similar to that disclosed at Figure 19 of Yamasaki, *et al.*, and also similar to that disclosed to the conventional internal voltage generating circuit illustrated at Figure 1 of the present specification. The voltage down converter VDC of Yamasaki, *et al.* generates an internal power supply voltage intVcc on an internal power supply line IVL according to a reference voltage Vref from a reference voltage generating circuit RFG (see Yamasaki, Figure 1 and page 5, paragraph [0066], lines 5-10). The internal voltage down converter VDC includes a comparator CMP that compares the reference voltage Vref with the internal power supply voltage intVcc on the internal power supply line IVL, and further includes a drive transistor DR that supplies current from an external power supply node EX to the internal power supply line IVL according to the output signal form the comparator CMP (see Yamasaki, Figure 1 and page 5, paragraph [0066], lines 10-17).

The driving circuit 2 of Yamasaki, *et al.* is connected between the reference voltage generating circuit RFG and the internal voltage down converter VDC (see Yamasaki, Figure 1). The driving circuit 2 of Yamasaki, *et al.* generates a voltage Vrfo that is substantially the same voltage level as the reference voltage Vref output from reference voltage generating circuit RFG (see Yamasaki, Figure 1 and page 5, paragraph [0068], lines 1-6). The driving circuit 2 is

activated in response to a test mode designating signal TE (see Yamasaki, Figure 1 and page 5, paragraph [0068], lines 6-11).

The test mode setting circuit 3 of Yamasaki, *et al.* activates/deactivates the test mode designating signal TE when a row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add are set to a predetermined combination of states (see Yamasaki, Figure 5A and page 7, paragraph [0092]).

However, there is no teaching or suggestion in Yamasaki, *et al.* that the test mode setting circuit 3 generates the test mode designating signal TE as an activated control signal when the row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add indicates that a number of data bits being processed by the semiconductor device is more than a predetermined number of bits. Further, there is no teaching or suggestion in Yamasaki, *et al.* that the test mode setting circuit 3 generates the test mode designating signal TE as an inactivated control signal when the row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add indicates that a number of data bits being processed by the semiconductor device is less than a predetermined number of bits. More specifically, there is no teaching or suggestion in Yamasaki, *et al.* that the address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add indicates that a number of data bits being processed by the semiconductor device is either more than or less than a predetermined number of bits. While the address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add of Yamasaki, *et al.* rise and fall during a test mode (see Yamasaki, Figure 5B), there is no teaching or suggestion that the change in state of the address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and specific address signal bit Add of Yamasaki, *et al.* indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the

number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 10.

Further, even if the test mode designating signal TE of Yamasaki, *et al.* is a control signal, there is no teaching or suggestion in Yamasaki, *et al.* of an internal voltage generating circuit being coupled to the control signal generating circuit for receiving the control signal, as claimed in independent claim 10. Specifically, there is no teaching or suggestion of voltage down converter VDC of Yamasaki, *et al.* being coupled to the test mode setting circuit 3. Moreover, the voltage down converter VDC of Yamasaki, *et al.* does not receive the test mode designating signal TE of Yamasaki, *et al.* Instead, the test mode designating signal TE of Yamasaki, *et al.* is applied to the driving circuit 2 of Yamasaki, *et al.* In addition, as described above, the voltage down converter VDC of Yamasaki, *et al.* is similar to a conventional internal voltage generating circuit, for example, the circuit shown in Figure 1 of the present specification. It therefore follows that the voltage down converter VDC of Yamasaki, *et al.* is different than Applicants' claimed internal voltage generating circuit.

In addition, while the driving circuit 2 of Yamasaki, *et al.* receives the test mode designating signal TE, the driving circuit 2 of Yamasaki, *et al.* is likewise different than Applicants' claimed internal voltage generating circuit. Specifically, there is no teaching or suggestion in Yamasaki, *et al.* of the driving circuit 2 being an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal, a switching circuit coupled to an output of the comparing circuit for receiving the control signal and for transmitting the comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, a driving signal control circuit for inactivating the driving signal when the control signal is activated, and an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in independent

claim 10.

In particular, the driving circuit 2 of Yamasaki, *et al.* does not comprise a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal, as claimed in claim 1. Instead, the driving circuit 2 includes a differential amplifier 2b that compares a receiving voltage Vrfo to a reference voltage Vref (see Yamasaki, Figure 1).

In addition, there is no teaching or suggestion of either the voltage down converter VDC or the driving circuit 2 of Yamasaki, *et al.* including a switching circuit coupled to both a control signal generating circuit and an output of a comparing circuit for receiving a control signal and for transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, as claimed in amended independent claim 10. Although the abovementioned voltage down converter VDC comprises a drive transistor DR, as noted in the Office Action at page 5, last line through page 6, line 8 and page 11, second paragraph, there is no teaching or suggestion in Yamasaki, *et al.* of the drive transistor DR receiving a control signal and transmitting the comparing signal as a driving signal when the control signal is inactivated, as claimed in amended independent claim 10. Instead, the drive transistor DR of Yamasaki, *et al.* is similar to the transistor P of driver D illustrated at Figure 1 of the present specification.

Sher likewise fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 10. In addition, Sher likewise fails to teach or suggest an internal voltage generating circuit comprising a comparing circuit for

comparing a reference voltage to an internal voltage to generate a comparing signal, a switching circuit coupled to an output of the comparing circuit for receiving the control signal and for transmitting the comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, a driving signal control circuit for inactivating the driving signal when the control signal is activated, and an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in independent claim 10.

With regard to the rejection of independent claim 23 based on the combination of Yamasaki, *et al.* and Sher, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or suggests a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 23, for reasons similar to those described above with regard to claim 10. In addition, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or suggests an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit that cuts off an external power voltage applied to the internal voltage generating circuit when the control signal is activated, a second switching circuit that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal is activated, and a third switching circuit including a CMOS transmission gate which transmits the

driving signal when the control signal is inactivated, as claimed in independent claim 23, for reasons similar to those described above with regard to claim 10.

Accordingly, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the invention set forth in the claims. Since the combination of Yamasaki, *et al.* and Sher fails to teach or suggest the invention set forth in the claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher are respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited.

If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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